

# IPID4all Doctorate Research Exchange with National University of Singapore

## Feedback report

*M. Sc. Alex Neumüller*  
*Next Energy*  
*Photovoltaics – New Technologies*  
*Carl-von-Ossietzky-Straße 15*  
*26129 Oldenburg*  
*GERMANY*

*Dr. Martin Vehse*  
*January 2016 – March 2016*  
*Interface characteristics of heterojunction solar cells*  
*with absorbers below 70 µm*

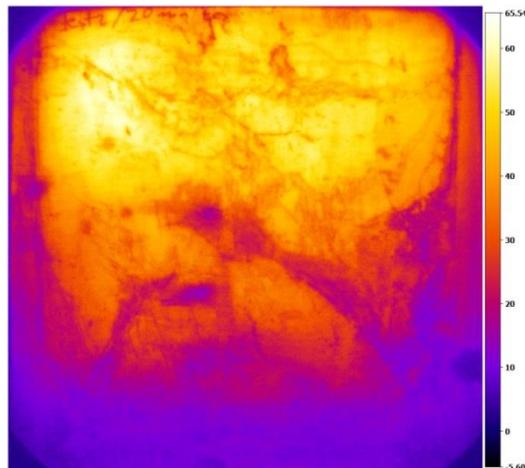
*National University of Singapore*  
*SERIS Institute*  
*Heterojunction Silicon Wafer Solar Cell*  
*Block E3A, #06-01*  
*7 Engineering Drive 1*  
*Singapore 117574*  
*SINGAPORE*  
*Dr. Thomas Müller*

### Introduction

The initial plan of my research activities was the development of high-quality passivation layers for monocrystalline silicon absorbers (c-Si) of thicknesses below 70 µm. Using our “new” approach (the paper will be submitted within the next month) to passivate c-Si wafers we wanted to see the effect of such passivation layers in comparison to thin c-Si wafers. Unfortunately, the ICP-PECVD tool was still under maintenance when I arrived so we needed to change the plan a little bit. Therefore I worked on the preparation of such ultra-thin wafers. Therefore I tried to develop an etching procedure for etching slurry cut wafers to thicknesses below 70 µm since nobody had the experience at the SERIS institute.

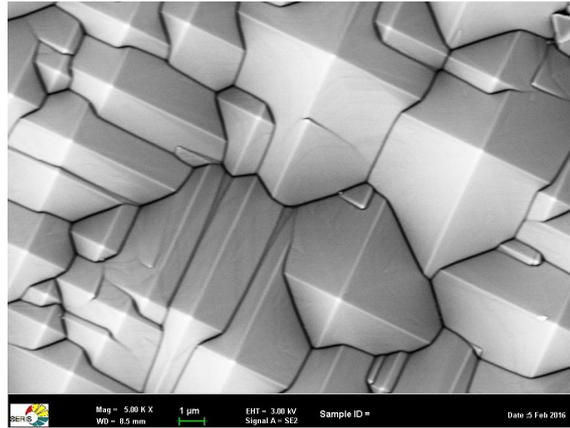
### Research Undertaken

At the SERIS institute, they have a very well equipped experimental lab. Besides the wet chemical bench, the photoluminescence (PL) setup, the SEM, 3D-microscope and lifetime tester were used. In this report, some of the measurements are depicted (compare Fig. 1, Fig. 2). To investigate the influence of the different etching/texturing steps on the bare c-Si wafers it was crucial to evaluate the etching rates (see Fig. 3).

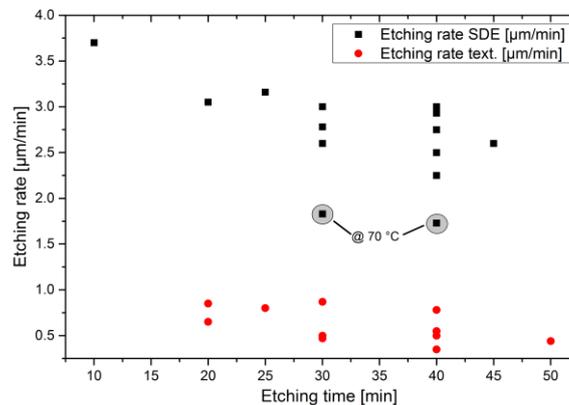


**Figure 1:** Photoluminescence with calibrated lifetime measurements.

Photoluminescence (PL) measurements (Fig. 1) show strong inhomogeneities. This could be due to the floating of the samples in the bath. Several wafers were fabricated and the PL spectra offered as a very deep insight into material properties, etching/texturing quality and in uniformity. In Fig. 2 the same wafer is measured using a SEM. The picture shows the pyramidal structure of the etched and textured wafers. It also shows a very smooth structure of the pyramids. If the processes weren't sufficiently etched and textured some “dirt” was visible especially between the pyramids.



**Figure 2:** SEM pictures of well textured silicon wafers for the purpose of high efficient heterojunction solar cells. The magnification of the picture is 5000x.



**Figure 3:** An overview over the different etching rates of all the conducted tests. Red points are indicating the etching rates of the texturing etching process while the black points are the SD-etched samples. The two highlighted points were SD-etched at 70 °C.

Figure 3 shows the etching rates during saw damage removal etching (SDE) and texturing for different etching times. It is obvious that with increasing SDE time the etching rate is decreasing due to reduced chemical concentration in the bath. This was one of the main issues during my staying. The researchers at SERIS just started to work on the wet bench and were quite inexperienced so we needed to stabilize and study these processes. As the texturing procedure was more established in the institute we obtained more stable and reproducible etching rates und texturing uniformities.

Batch	SDE [min]	Weight [g]	Thick [μm]	Alk. text. [min]	RCA1 [min]	HF [min]	RCA2 [min]	Weight [g]	Thick. [μm]
1	30	8.09 ± 0.40	145 ± 7	50	10	1	10	6.84 ± 0.34	123 ± 6
2	40	7.31 ± 0.37	131 ± 7	40	10	1	10	6.17 ± 0.31	111 ± 5
3	40	4.65 ± 0.23	83 ± 4	20	10	1	10	3.88 ± 0.19	70 ± 4
4	30	6.52 ± 0.33	117 ± 6	40	10	1	10*	5.27 ± 0.26	95 ± 5
5	40	4.97 ± 0.25	90 ± 5	30	10	1	10	4.19 ± 0.21	76 ± 4
6	40	5.54 ± 0.28	100 ± 5	40	10	1	10	4.76 ± 0.24	86 ± 4

**Table 1:** Etching steps and thicknesses are noted.

# IPID4all Doctorate Research Exchange with National University of Singapore

## Feedback report

At SERIS we produced 6 different wafer batches (see Tab. 1). The plan was to take the samples back home and to finish the originally planned depositions and further experiments in my home institute. Thin a-Si:H, a-SiO:H, a-SiON:H and a-SiOC:H layers will be deposited with a von Ardenne PECVD tool and the different amorphous silicon alloys will be analyzed. Further argon and hydrogen post-deposition plasma treatments will be applied to improve and study the influence of such post-deposition applications.

### Personal Experience

Although the planned experiments couldn't be finished or started due to some technical issues my supervisor and the staff found an adequate and interesting task for me. I learned a lot from a different point of view, especially because I never worked at a wet bench with chemicals. The staying in Singapore was also very beneficial for my work structure and I used effectively the time to study the literature and evaluated all the measurements I did for my Ph.D. My supervisor Thomas Müller was very nice and tried to help me as much as possible. He also offered me a collaboration if I should need further samples or anything else. I am quite confident that in the near future, I will go back and join the research group for other research activities.

From the personal point of view, it was very nice to stay in Singapore and to experience a different way of life and to meet people from all over the world. I am sure that some friendships will last forever.

### Conclusions

In conclusion, one can say, that especially regarding stable processes and etching rates several tests should be conducted. Due to the thick Comtec bare wafers, the etching times are quite a height and of course the consumption of chemicals as well. Most preferably thinner slurry cut or even diamond cut wafers should be used to achieve thicknesses below 100 µm. Regarding our results a RCA1 together with RCA2 cleaning steps are highly recommended and the drying process should be optimized as well. In the near future, the IPA dryer should work and especially the production of thin and ultra-thin wafers would benefit from this drying technique.

Personal conclusion: I would recommend a research stay in Singapore to anybody. The financial support by the Singaporean government is huge and the labs and other facilities are well equipped. The opportunity to meet people from so many different cultures is fascinating and inspired me a lot..

### Outlook

- o Publications are planned. I am now finishing my last paper for my Ph.D. and after that, I start to write on the results obtained with the support of this program.
- o I am planning to start a close collaboration between the research group at Next Energy and the SERIS institute.



Deutscher Akademischer Austausch Dienst  
German Academic Exchange Service

GEFÖRDERT VOM



Federal Ministry  
of Education  
and Research



Bundesministerium  
für Bildung  
und Forschung